# Synchronize Method for FSM Asynchronous Inputs

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**Rezumat.** Sinteza şi implementarea sistemelor logice secvenţiale FSM, se poate realiza mult mai uşor folosind circuite integrate MSI şi LSI. Cu cât funcţiile realizate de acestea sunt mai complexe, cu atât logica combinaţională de implementare a sistemului devine mai simplă. Atunci când sistemul este alcătuit din semnale de intrare atât sincrone cât şi asincrone, înainte de utilizarea în sistem, acestea trebuiesc sincronizate. În această lucrare este propusă o metodă de realizare a sincronizării intrărilor asincrone a unui sistem secvenţial.
**Keywords:** Finite State Machine, Transition Matrix, Counter, Logic Primitive, Medium Scale Integration, Lower Scale Integration, CBB, Temporal Diagrams, FSM Graph, FSM Transition Table.

## 1 Introduction

Synthesis of the sequential digital automata can be reduced to a combinational synthesis, specified CAD doing it in 2 steps: first, synthesis using primitives (logic gates) and second, using technological implant.

When a sequential finite automata is drived by the internal system clocks from one part and by out signals, from the other part, asynchronous between them, there can appear functional hazards. This, because of time delay between automata clocks signals and out signals.

So, the time set-up ($t_{set\text{-}up}$) and time hold ($t_{hold}$) finite automata variables can't be respected. There can be obtained wrong short signals who will affect the normal functionality of finite automata. This paper presents one method to avoid these situations.

## 2 Synchronisation Method for FSM Asynchronous Inputs

Let's consider that we have one big finite automata (A) that is composed by two smalls finite automata (A1,A2), like in figure 1.

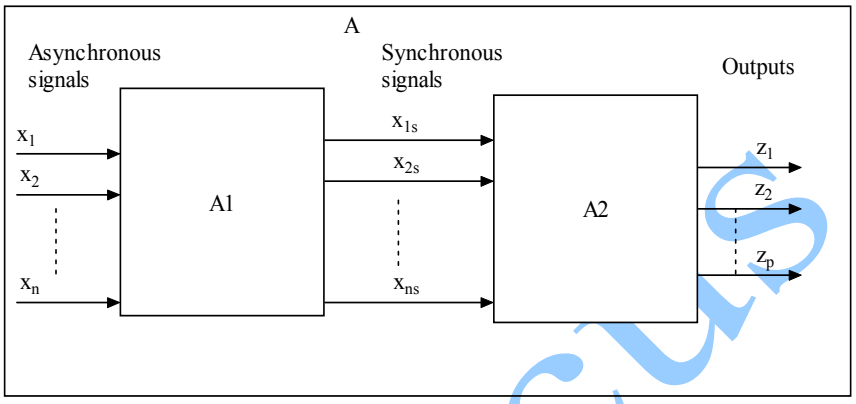


*Figure 1*

$X_1$, $X_2$… $X_n$ represents the input signals for A1 finite automata.
$X_{1s}$, $X_{2s}$… $X_{ns}$ represents the output signals from A1 finite automata and input signals for A2 finite automata. These signals are synchronized by a digital clock signal h1, figure 2.
$Z_1$, $Z_2$… $Z_p$ represents the output signals for A2 finite automata.

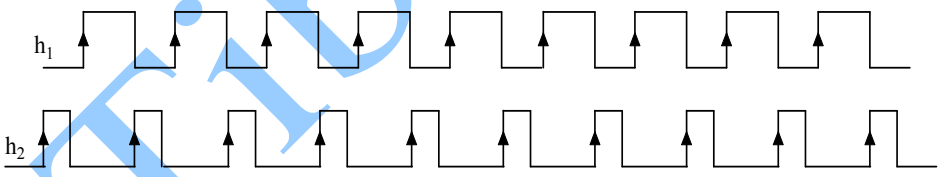


*Figure 2*

The $h_2$ digital clock (active on positive edge) represents the input driving clock for A2 finite automata.

Figure 3 presents the digital implementation of A finite automata with all inputs signals synchronized by $h_1$ digital clock.

On figure 3 it's observed that $X_1$, $X_2$… $X_n$ asynchronous input signals are synchronized by using CBB $D_{s1}$, $D_{s2}$… $D_{sn}$ circuits. These circuits are driving by a $h_1$ digital clock. It has the ability to synchronize all the inputs, the circuits outputs are synchronized signals driving by a $h_1$ digital clock signal.

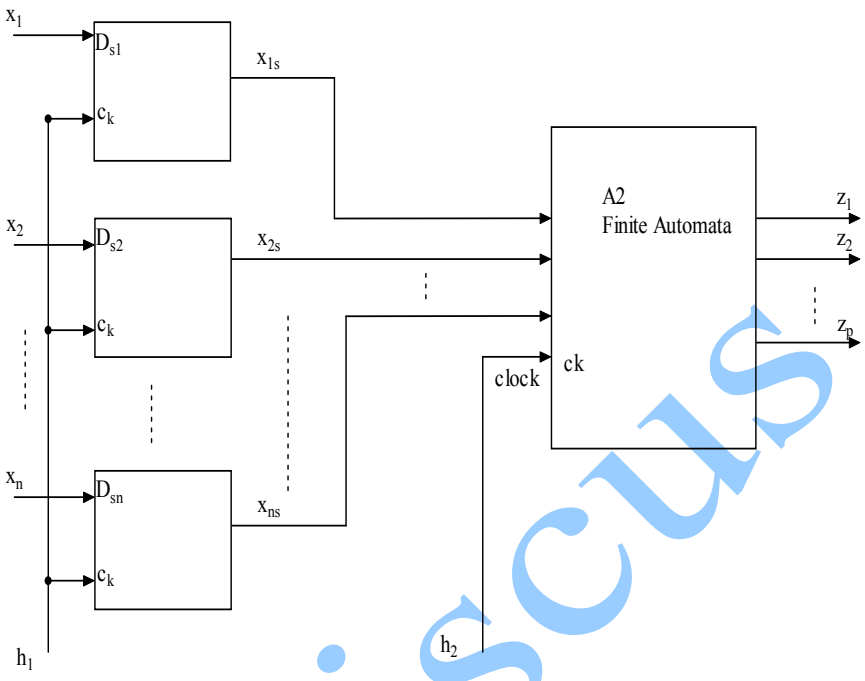


*Figure 3*

The A2 finite automata digital clock signal is Ck= $h_2$ . $Z_1$, $Z_2$… $Z_p$ represents the A2 finite automata output computed results.

## 3 Example of Synchronisation Method for FSM Asynchronous Inputs

We will consider finite automata fluence state graph like in figure 4.

The $x_1$, $x_0$ are asynchronous input signals of finite automata and $z_1$, $z_0$ represents the output signals from finite automata.

It needs to progress with a T time period when $x_1$ or $x_0$ inputs signals are presented. So, we will introduce a T period time clock and the finite automata command will be driving by $h_2$ .

But $x_1$ or $x_0$ input signals are asynchronous one by one, this can be obtained a very small time period who can't be counted by the finite automata. To avoid this situation we need to synchronize these input signals with two CBB D circuits.

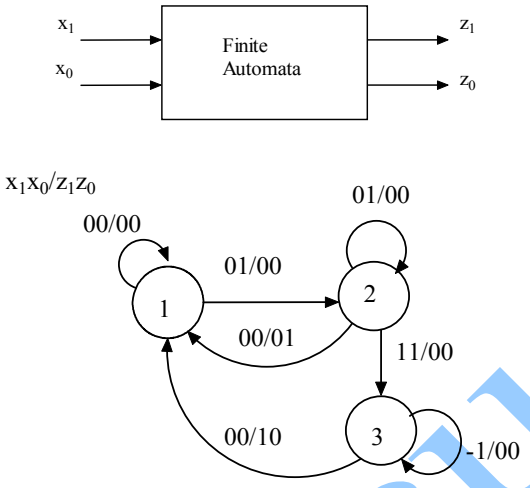


*Figure 4*

Figure 5 shows these two synchronization clock, $h_1$, $h_2$ and the digital design of this finite automata.

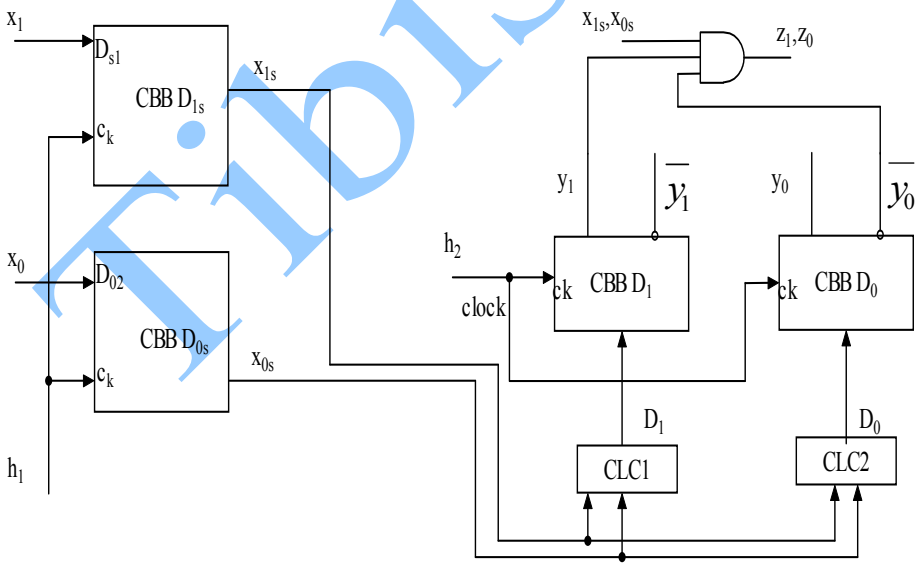


*Figure 5*

The $h_1$ clock synchronize external input signals, recopy them on two CBB D circuits (CBB $D_{1s}$,CBB $D_{0s}$). Synchronizations signals $x_{1s}$, $x_{0s}$ has some delay than the $x_1$, $x_0$ input signals. The $h_2$ represents the driving clock input signal for CBB $D_1$ and CBB $D_0$ circuits, figure 5.

## 4 Conclusions

To synchronize any number of asynchronous signals it will need to use the same number of CBB D circuits or a memory register, figure 6.

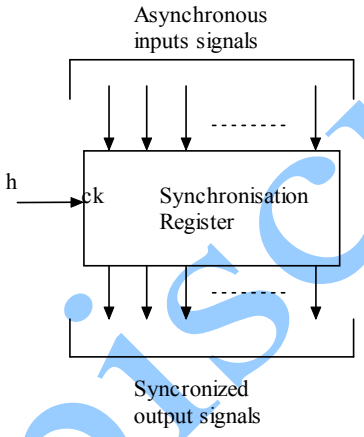


*Figure 6*

On every sequential system, finite automata system, before of using the asynchronous input signals we need to synchronized them with a digital clock input signal.

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