# An Overview of the Asynchronous Digital Systems – Part 1

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**Abstract**: Implementation methods for the digital asynchronous systems use different predefined models like self timed circuits, speed independent circuits, delay insensitive circuits, handshake protocol implementation in asynchronous systems.
**Keywords**: Asynchronous digital systems, self timed, speed independent, delay insensitive, handshake.

## 1.Introduction

In this paper, the author presents an overview of the asynchronous digital systems like self timed, speed independent, delay insensitive, handshake protocol implementation in digital asynchronous systems.

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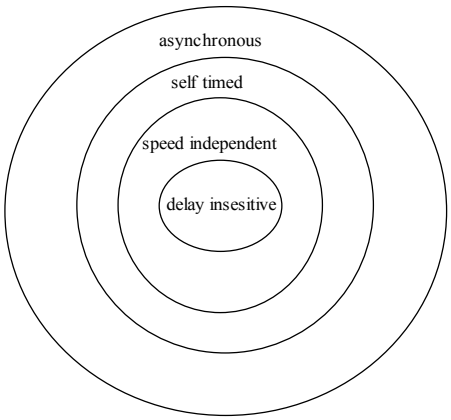


Figure 1

A delay insensitive circuit works correctly indifferent of the propagation timing delays through wires and circuits. This concept was firstly introduced by Clark and Molnar, [Cla67].

A speed independent circuit works correctlly indifferent of the propagation timing delays through circuits. The wire has a specific delay propagation values. This concept was firstly in introduced by David Muller [Mul65].

A self timed circuit uses a temporized elements where the wires delay propagation timing are known or neglijable. Using the time informations values, they are builded like speed independent circuits, [MC80].

The asynchronous sequential system represents the general category, [Ung69], they haven't a localy clock signal, they are running using internally timing values. The latches and flip-flops circuits works asynchronous, [Clu86], they have the time set-up and time-hold predefined values.

## 2. Data communication

When two digital systems comunicates, the receiver system must know when the data is valid. In asynchronous digital systems, the receiver must be trigered by the sender when the transmition of data starts or ends. This is done using the ACK signal (acknowledge signal). The active system block initiate the communications and the passive system block responds to the actions initiating by the active system block. The concept used in the design of the asynchronous digital systems is named handshake, figure 2.

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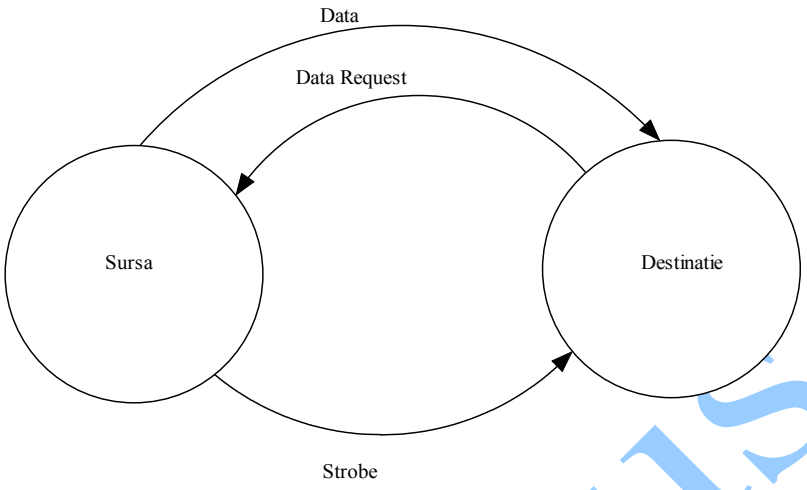


Figure 2

The data transfer is starting by the sender by activation of the Data and Strobe signals, the acknowledge process is done by the receiver when the Data Request signal is generated, figure 3.

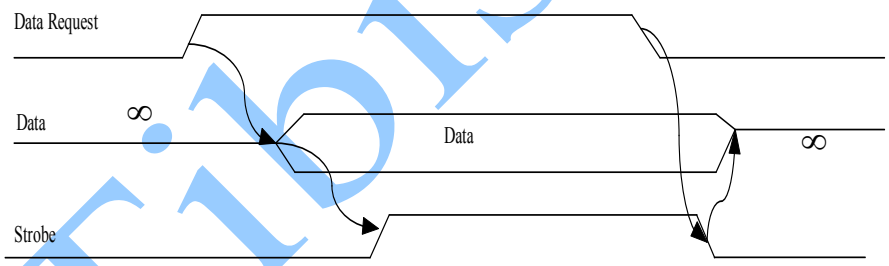


Figure 3

When the data transfer is started by the sender, figure 4, 5.

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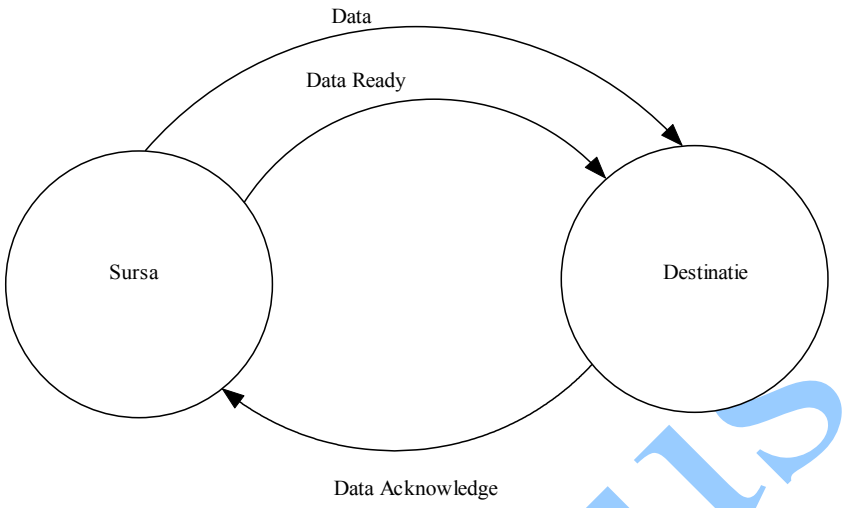


Figure 4

In asynchronous digital systems there are no differences between level and edge signal transitions, figure 5.

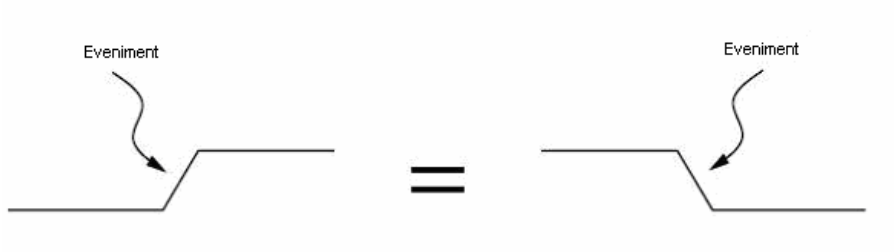


Figure 5

When the hanshake process is done using the level signals, an event is recognized when the signal change its value from 0 to 1 and 1to 0, as presented in figures 6, 7.

## Conclusions

Using the predefined circuits models in implementation of asynchronous digital systems means avoid errors and digital hazard situations. The digital asynchronous system will run correctly, according with the specifications.

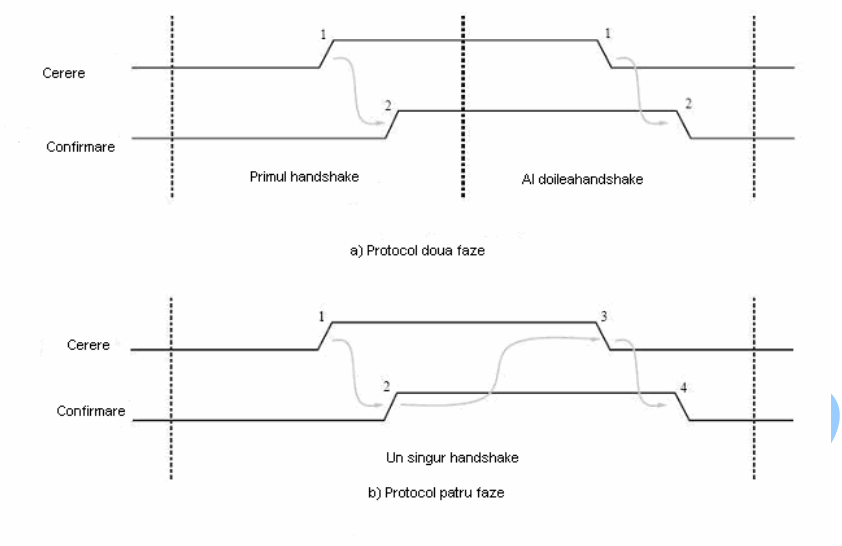


Figure 6

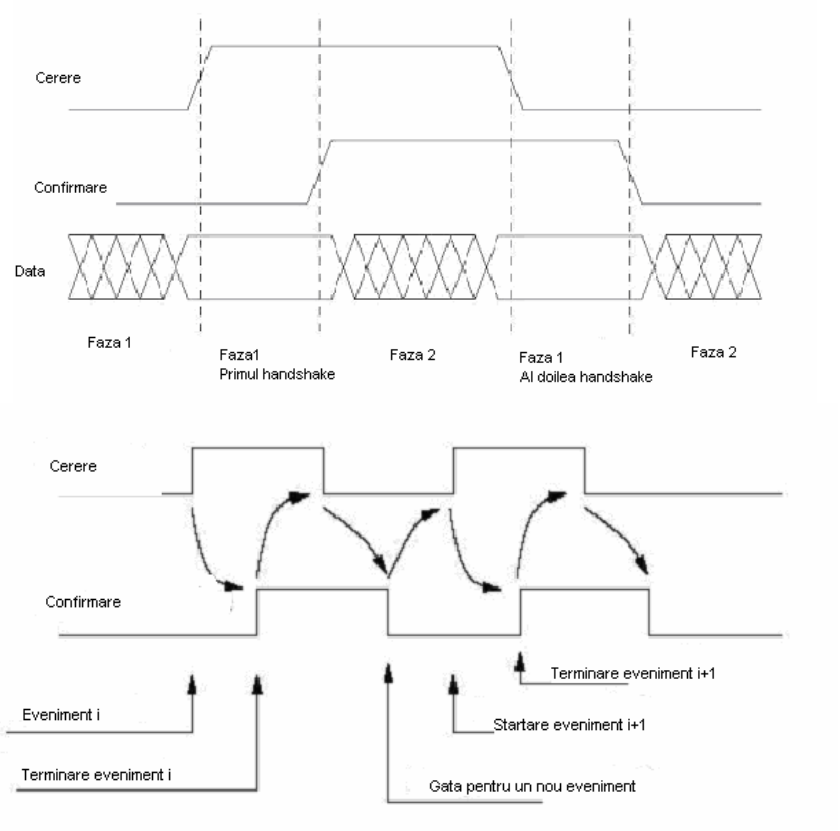


Figure 7

## References

[Cla67] W. A. Clark, *Macromodular computer systems,* In Proceedings of the Spring Joint Computer Conference, AFIPS, April 1967

[Clu86] E. J. McCluskey, *Logic Design Principles: with emphasis on testable semicustom circuits*, Prentice Hall, Englewood Cliffs, NJ, 1986

[Mul65] R. E. Muller, *Switching Theory. Volume II: Sequential Circuits and Machines*, John Wiley and Sons, New York, NY, 1965.

[MC80] C. Mead, L. Conway, *Introduction to VLSI Systems*, Addison Wesley, Reading, MA, 1980, C.L.Setiz, System Timing

[Ung69] S. H. Unger, *Asynchronous Sequential Switching Circuits. Wiley Interscience*, New York, NY, 1969

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