An Overview of the Asynchronous Digital Systems – Part 2

Assist.Prof. Grigore Mihai TIMIS, Ph.D., Dipl.Eng.
"Gh.Asachi" Technical University of Iasi,
Automatic Control and Computer Science&Engineering Faculty
Computer Science and Engineering department
mtimis@cs.tuiasi.ro

Abstract: Implementation methods for the digital asynchronous systems use different predefined models like self timed circuits, speed independent circuits, delay insensitive circuits, handshake protocol implementation in asynchronous systems.
Keywords: Asynchronous digital systems, self timed, speed independent, delay insensitive, handshake.

1. Introduction

In this paper, the author presents an overview of the asynchronous digital systems like self timed, speed independent, delay insensitive, handshake protocol implementation in digital asynchronous systems.

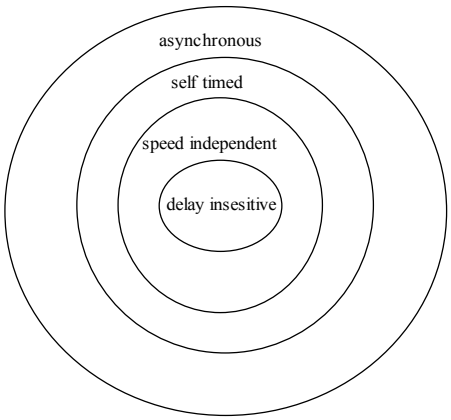

Figure 1

A delay insensitive circuit works correctly indifferent of the propagation timing delays through wires and circuits. This concept was firstly introduced by Clark and Molnar, [Cla67].
A speed independent circuit works correctlly indifferent of the propagation timing delays through circuits. The wires have specific delay propagation values. This concept was firstly in introduced by David Muller [Mul65].
A self timed circuit uses a temporized elements where the wires delay propagation timing are known or neglijable. Using the time informations values, they are builded like speed independent circuits, [MC80].
The asynchronous sequential systems represent the general category, [Ung69], they haven't a localy clock signal, they are running using internally timing values. The latches and flip-flops circuits works asynchronous, [Clu86], they have the time set-up and time-hold predefined values.

2. Circuits Models

A completed digital circuit represents a system with two parts: the digital circuit and the system's environments where it runs. A digital circuit model describes how the logic gates delays are displayed.

3. Delay Models

There are two delay types: stray delay which inherit the physical propreties of any circuits, and delay elements which are added by the designers.
The delay elements can be classified in pure delays and inertial delays. The pure delay propagates the signal from the output after a fixed time period, noted with d, figure 1. The pure delays can be implemented using buffers.

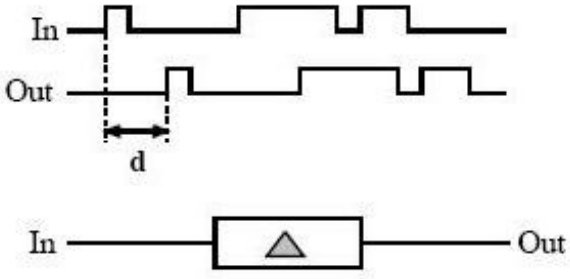

Figure 1

The inertial delays propagates only the signals which are stabile for a period of time, these are delayed with a fixed time noted with d.
Inertial delays are used for the glitch free filtering, figure 2.

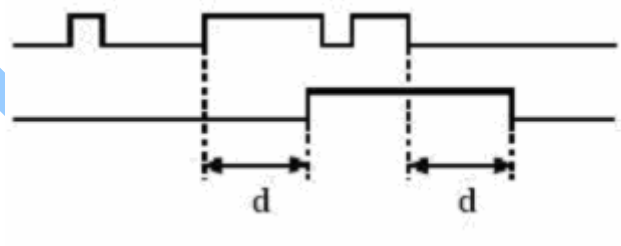

Figure 2

The asymetric delay has different values for the propagation timing.
The signals which had asymteric delays has a propagation delay named d_h when the signal is high and d_l when the signal is low, figure 3.

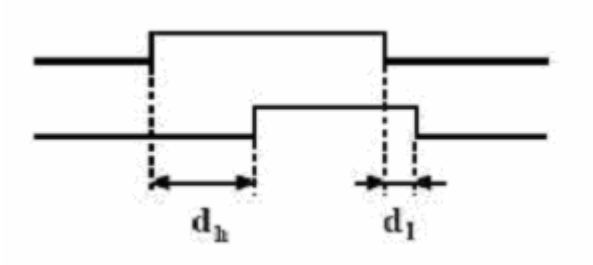

Figure 3

The delays generated by the wire delays are implemented in the circuit's inputs. The gate delays are represented on the output of the circuits.
The circuits that uses delays in the inputs and outputs are the most difficult to be implemented, figure 4.

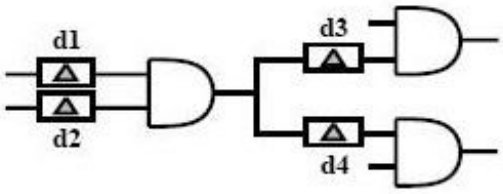

Figure 4 – wire delays

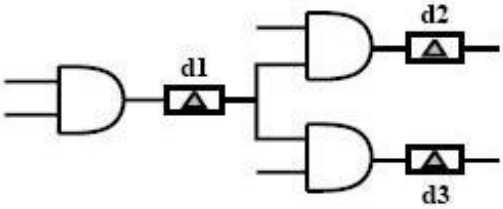

Figure 4 – logic gates delays

4. Circuits models and systems

The input-output mode didn't take into account different forced time restrictions. If this is taken into account, the system runs in fundamental mode with timed circuits. The circuit model describes the stary delay and delay elements, handle delays, bounded delays, unbounded delays, [Cla67].
When a command was started the digital system may know on which period of time was started. This is done using an acknowledged – ACK – signal.

This signal shows that the sended signals were received and more data can be sended on.

Conclusions

Using the predefined circuit models in implementation of asynchronous digital systems means avoid errors and digital hazard situations. The digital asynchronous system will run correctly, according with the specifications.

References

[Cla67] W. A. Clark, *Macromodular computer systems,* In Proceedings of the Spring Joint Computer Conference, AFIPS, April 1967

[Clu86] E. J. McCluskey, *Logic Design Principles: with emphasis on testable semicustom circuits*, Prentice Hall, Englewood Cliffs, NJ, 1986

[Mul65] R. E. Muller, *Switching Theory. Volume II: Sequential Circuits and Machines*, John Wiley and Sons, New York, NY, 1965.

[MC80] C. Mead, L. Conway, *Introduction to VLSI Systems*, Addison Wesley, Reading, MA, 1980, C.L.Setiz, System Timing

[Ung69] S. H. Unger, *Asynchronous Sequential Switching Circuits. Wiley Interscience*, New York, NY, 1969