An Overview of the Asynchronous Digital Systems – Part 3

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Abstract: Implementation methods for the digital asynchronous systems use different predefined models like self timed circuits, speed independent circuits, delay insensitive circuits, handshake protocol implementation in asynchronous systems,C Muller circuits.
Keywords: Asynchronous digital systems, self timed, speed independent, delay insensitive, handshake, C Muller.

1. Introduction

In this paper, the author presents an overview of the asynchronous digital systems like self timed, speed independent, delay insensitive, handshake protocol implementation in digital asynchronous systems, C Muller circuits.

A delay insensitive circuit works correctly indifferent of the propagation timing delays through wires and circuits. This concept was firstly introduced by Clark and Molnar, [Cla67].

A speed independent circuit works correctlly indifferent of the propagation timing delays through circuits. The wires have a specific delay propagation values. This concept was firstly in introduced by David Muller [Mul65].

A self timed circuit uses a temporized elements where the wires delay propagation timing are known or neglijable. Using the time

information values, they are built like speed independent circuits, [MC80].

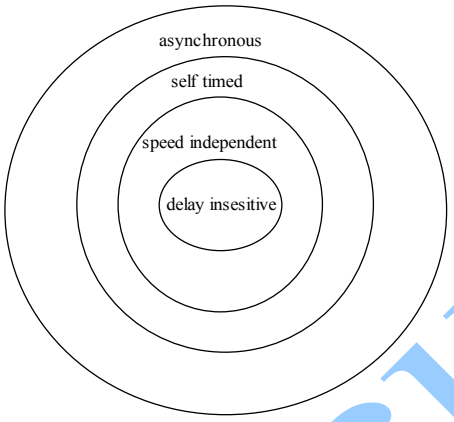


Figure 1

The asynchronous sequential systems represents the general category, [Ung69], they haven't a localy clock signal, they are running using internally timing values. The latches and flip-flops circuits works asynchronous, [Clu86], they have the time set-up and time-hold predefined values.

2. Delay insensitive circuits. C Muller circuits

A delay insensitive circuit has arbitrary delays for wires or logic gates. A delay insensitive circuit has macromodule blocks and the interconnection between them. Every macromodule block must be designed do not influence the stability of the entire digital system. The hardware logic design can be much harder to do because of the acknowledge ACK signal, [Huf54], [JJ96].

In this case is much better to use the Muller C logic gate, figure2.

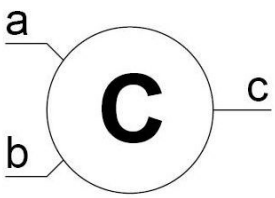
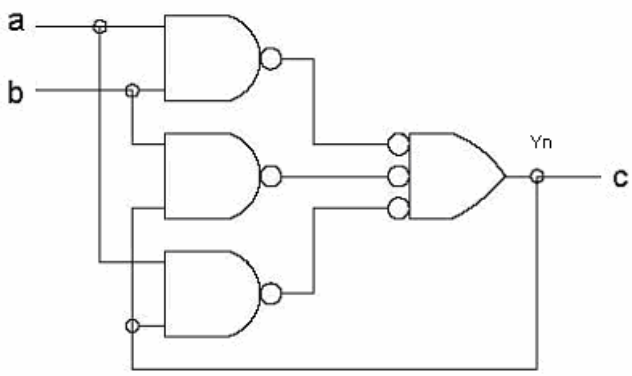


Figure 2

The internal C Muller logic gate design and the truth table are described in figure 3.



a b	c
0 0	0
0 1	C_{n-1}
1 0	C_{n-1}
1 1	1

Figure 3

The equation for the C Muller logic gate is $c = \bar{a} \cdot b \cdot c_{n-1} + a \cdot \bar{b} \cdot c_{n-1} + a \cdot b$
If used the noation c=yn+1, the C Muller logic gate equation is $y_{n+1} = \bar{a} \cdot b \cdot y_n + a \cdot \bar{b} \cdot y_n + a \cdot b$, the truth table is in figure 4.

a b y_n	y_{n+1}
0 0 -	0
0 1 -	y_n
1 0 -	y_n
1 1 -	1

Figure 4

When (abyn =00-) and (abyn=11-) it's done the write operation and when (abyn=01-) şi (abyn=10-) it'sdone the hold operation. The C Muller logic gate represents a logic latch circuit.

The delay in sensitive circuits are used as control circuits. A different delay model is represented by the speed independent circuits. It counts only the delays through logic gates, the wire delays aren't taken into account. A speed independent circuit runs good indifferent by the delays through logic gates.

The bounded delay means that the delay for every logic gate must be less than a maximum setted value. This model is common used in digital asynchronous systems.

A self timed circuit instantaneous calculates the value for a logic gate and after a delay it assigns it to the output, [Dil89].

3. Data valid protocol

In the asynchronous communication systems a wide range of protocols exists, figure 5, 6.

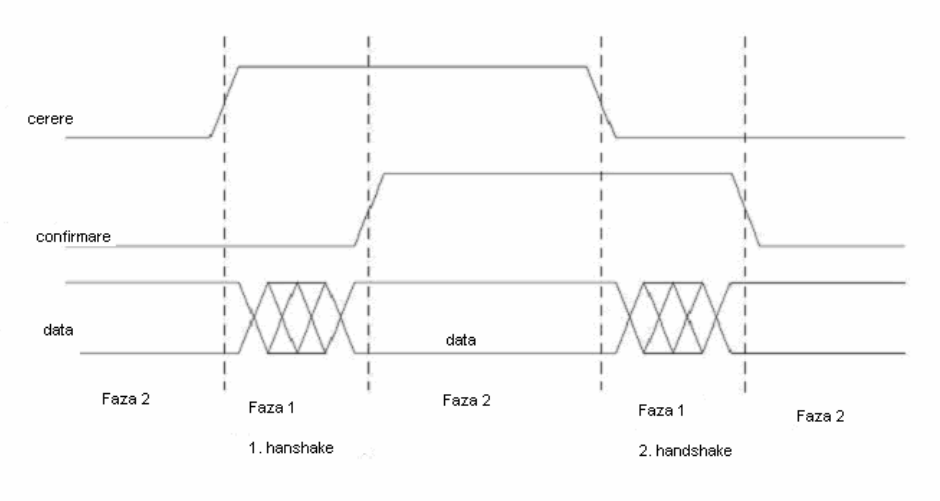


Figure 5

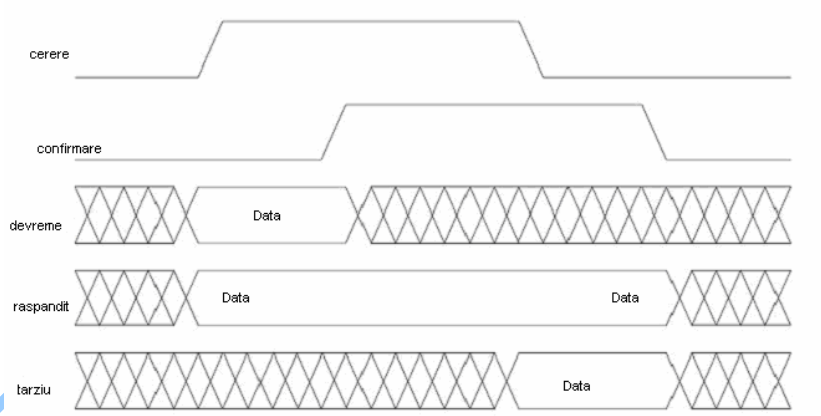


Figure 6

In the broad protocol, the data must be valid during the handshake protocol. In the late protocol, data must be valid between the negative transitions on the request, acknowledge signals.

The four phase pull chanell with aditional protocols for the datas are ilustrated in figure 7.

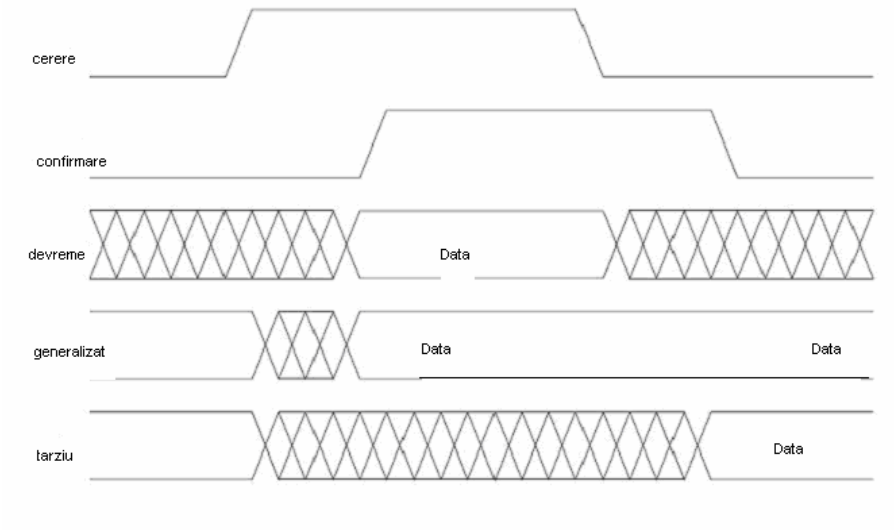


Figure 7

In this case, the receiver is the active part which request datas from the sender. For the early protocol, datas must be valid between the positive signals from the sender and the negative signals from the receiver.
For the broad and late protocols, data must be valid between hanshake processes.

Conclusions

Using the predefined circuit models in implementation of asynchronous digital systems means avoid errors and digital hazard situations. The digital asynchronous system will run correctly, according with the specifications.

5. References

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