DESIGN & SIMULATION OF LOW POWER ANALOG TO DIGITAL CONVERTER FOR MEDICAL APPLICATIONS

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***ABSTRACT*:** Analog to Digital converters (ADC) are key design blocks in modern communication systems for high efficiency medical applications. In this work, a design of Analog to Digital converter for pressure sensor application has been presented. The main purpose of this research is to develop an accurate system block for measuring temperature signals. This work presents a new circuit architecture concept with implementation of circuit blocks. This architecture uses a modified dynamic comparator for comparing a supplied analog input voltage and a reference voltage. This work proposed different technique to implement low power, high-resolution A/D converter that can be used for biomedical applications and does not employ any component trimming or adjustment. There may be less power dissipation because this proposed ADC needs only one additional operational amplifier and a comparator compared to traditional one A/D architecture. This architecture is simulated at 0.35µ tsmc technology using Mentor Graphics tool at 3.3V power supply. Advantages and disadvantages of the architecture are discussed. Simulated results matched the proposed techniques.

KEYWORDS: pressure sensor, sensor network, data converter, operational amplifier, power efficiency, enabling technologies.

I. INTRODUCTION

The fast realization of advance MOS fabrication technology needs more signal processing functions which are implemented for lower power consumption and higher yield. It generated a high demand for low power, low voltage ADCs for sensor application. High efficiency Analog to Digital converters with very high sample/s rate and maximum bits of linearity have been implemented exclusively using few components [C+13], and their uses are of great importance for high-performance medical and instrumentation applications.

The applications of ADCs are applicable as many electronic systems that used to be entirely analog have been implemented using digital electronics. Examples of such applications include digital telephone transmission, cordless phones, transportation, and medical imaging. Furthermore, ADCs have found their way into systems that would normally be considered as being entirely digital as these digital systems are pushed to higher levels of performance. [HR13][C+12] Data storage is one example of such a system. We can say that Analog-to-digital converters (ADCs) are key design blocks in modern Microelectronic systems. This ADC can be used for important applications such as green environments, atmosphere measurement and control, smart conveyance.

Recent inventions provided very effective and practical applicable ideas in different areas of network sensor and computer science. The use of sensor nodes is numerous to examine and measure a particular at various locations.

This type of sensor can be used for temperature, pressure, environmental, sound, and other. These applications also rely on the battery strength. Practically, this low-power circuits and networking technologies make such sensors applicable on very small batteries and can be active for long durations in years. [***08][CM13]

Recent research proposed efficient low- power coding [CM13, A+07] for wireless sensor networks, which emphasized on power consumptions reduction of various communications protocols and gives significant contribution.

This work is such an effort to apply circuit techniques to implement a low power, high-resolution A/D converter can be used in medical applications, pressure sensor, temperature etc.The proposed converter design is capable to reduce the power consumption for bio medical application. The converter also enhances the battery life of medical devices and wireless sensor nodes. [HR12][HR13]

This converter design decreases the capacitor charging voltage and also reduces the number of complex circuits in one conversion cycle, so this increased energy effectiveness gives us large power

savings without any sacrifice in terms of data efficiency, gain. The power saving emphasize in the new technology can also be appropriate in intense data conversion. The low power converter will be the effective elements in promising. Section II discusses the ADC's architecture and details the simulation of its building blocks. Experimental results are shown in section III and section IV of this paper.

II. CIRCUIT TECHNIQUE USED IN ADC

The method include for the steps of A/D-converting and sampling the analog input signal during a sampling period generating a given bias voltage corresponding to digital input signal obtained during the sampling period and applying the given bias voltage to a next-stage capacitor to be connected with the output terminal of the A/D converter circuit. In this A/D conversion method described above, the initial value setting period maybe set between the sampling period and the amplification period. Low power dissipation and high performance of static characteristic have been obtained by using dynamic comparator techniques. The ADC prototype presented in this work made use of circuit-driven techniques the presentation focuses on highlighting the circuit techniques employed in low-voltage ADCs while identifying their advantages and disadvantages.

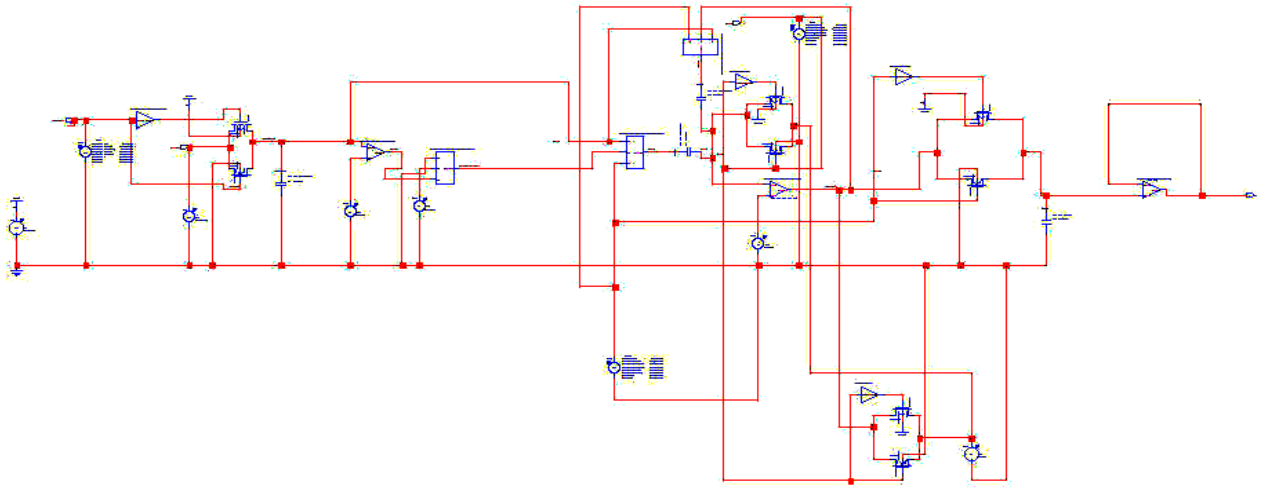


Fig. 1 Block diagram of 1 bit ADC

Proposed low power Technique

One distinct attribute between the traditional technique and the implemented technique is area savings. Here with the use of this Technique we are saving area, power consumption and increasing speed also. The idea behind the charge sharing technique is that after the current stage generates the output, the charge on the feedback capacitor is reused for the following stage instead of being thrown away.
A reference voltage V_{ref} is subtracted from the doubled input, and the residue voltage is compared with zero. If positive, the bit is ONE and the residue is sampled by the following stage. However, if negative, the bit is ZERO and the reference voltage is added back to the residue by switching back to the ground before it is sampled by the following stage.
Now we can say that if speed is the only restriction, the power consumption can be decrease by scaling down the capacitor size.

Description of Sub Building blocks

This function can be designed by using a charge-capacitor circuit as shown in Fig.2 which requires only two identical capacitors. Input is sampled in the sampling mode at the bottom plates of capacitors. In the next, capacitors are connected in the op-amp feedback paths; the basic operation includes sampling the signal on the sampling capacitor and transferring the signal charge onto the feedback capacitor.
In this way, all building blocks like low voltage comparator, shift register, sample and hold functions can be implemented with reducing building blocks. This method is mostly used in the S/H circuit. It can realize high speed because the feedback factor can be much larger than that of the previous configuration.

Additional Description of Design methodology

Other important requirements for the designing of ADC configuration like gain margin, slew rate, and mosfet resistances. As required by specifications we can set by the system.

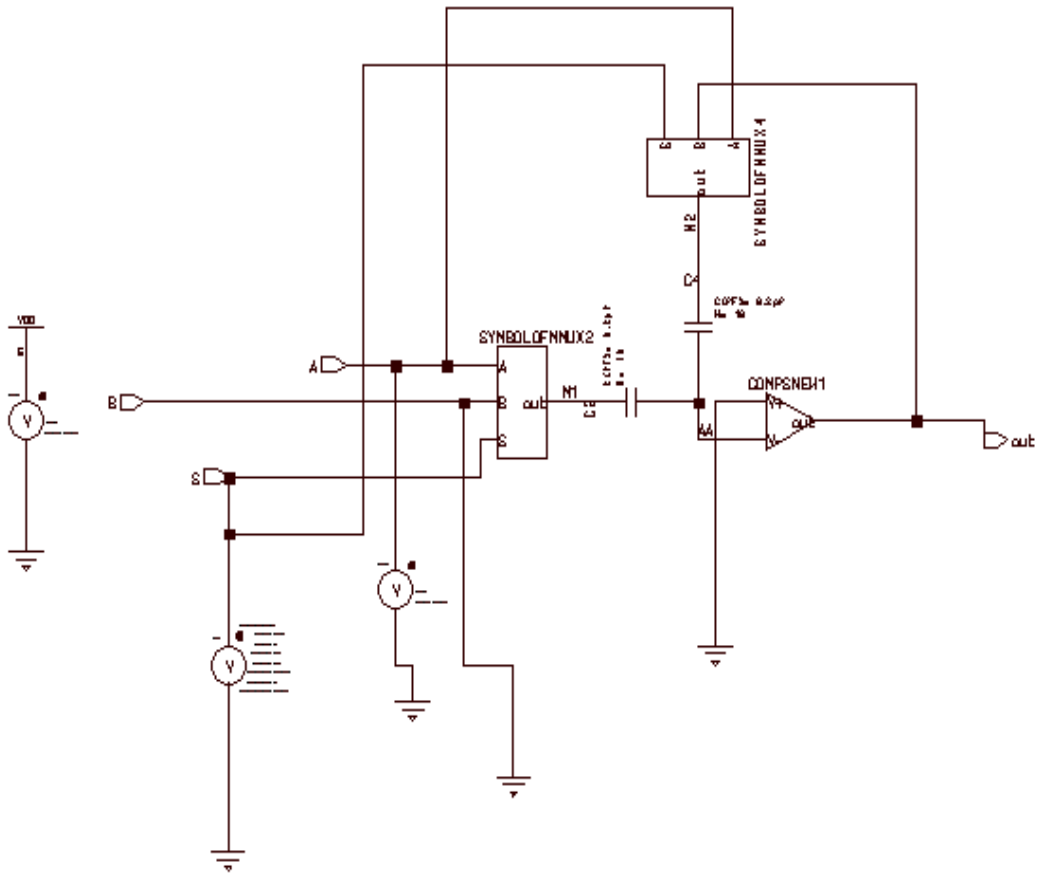


Fig. 2 Design methodology

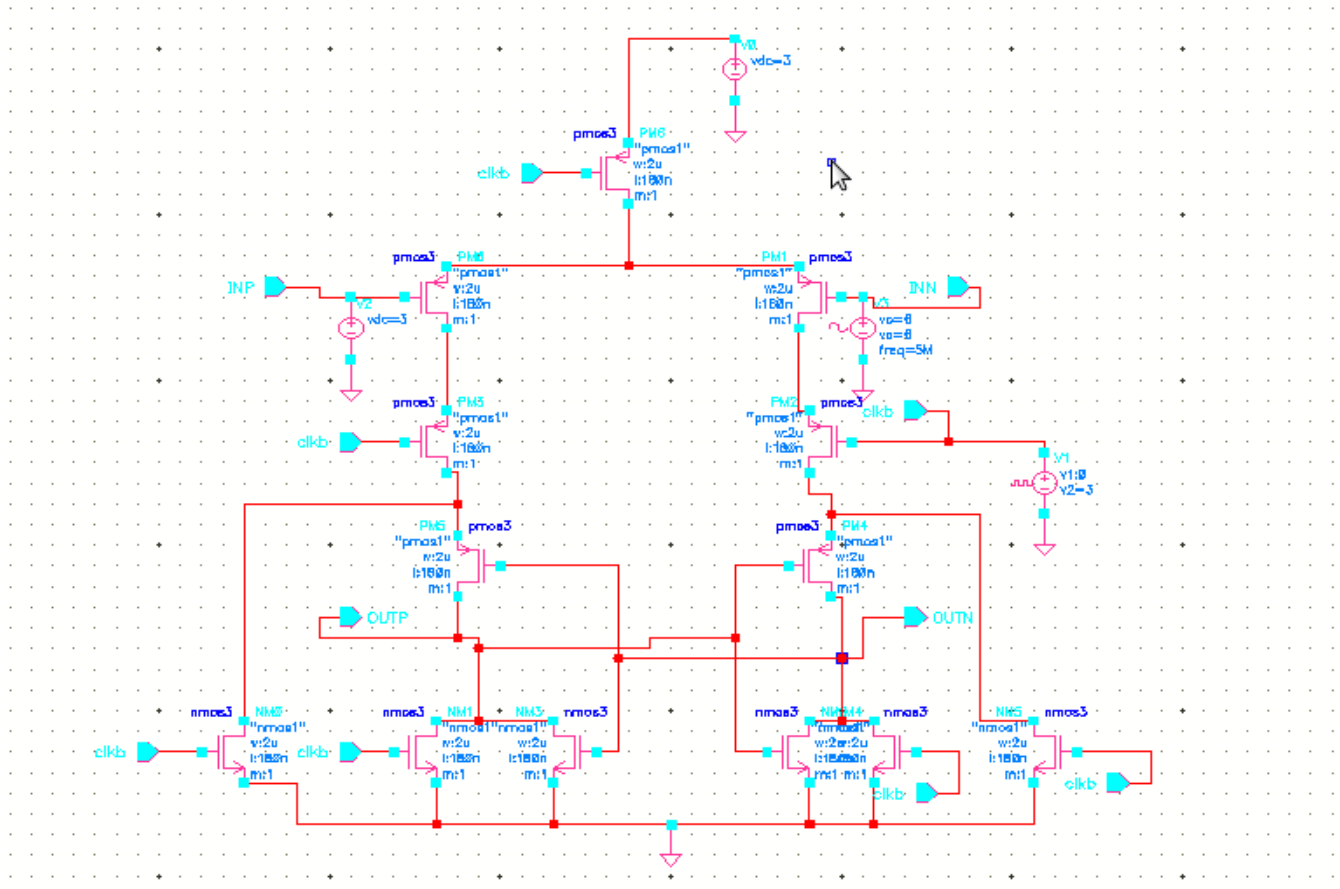


Fig.3 Schematic of Dynamic Comparator

In the multiply-by-two circuit of Figure 2 the offset does not affect the signal because it is sampled on the input capacitors by connecting the op amp in a unity-gain configuration.

However, differential charge injection and displacement current into the op-amp summing nodes generate a feed through error when the MOS switches charging the op-amp summing nodes are turned off.

The power dissipation of the single-transistor op amp SC circuit can be found by relating its bias current to the given settling requirement. The achievable time constant can be found for the given sampling/feedback capacitor values, current density, and load capacitance. To validate the design of the comparator and obtain its performance specifications, a number of Spice simulations were performed. The results obtained from these are now discussed. Then, the simulation results obtained for the S/H circuit dynamic comparator, operational amplifier will be used to calculate the conversion speed of the ADC.

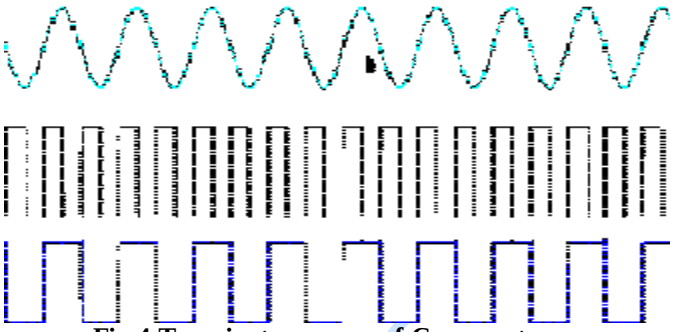
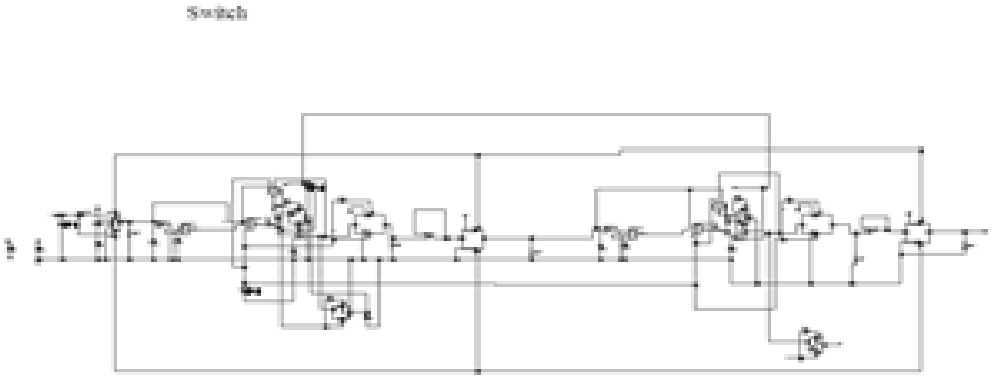


Fig.4 Transient response of Comparator

Cascading of I bit ADC



III. EXPERIMENTAL RESULTS

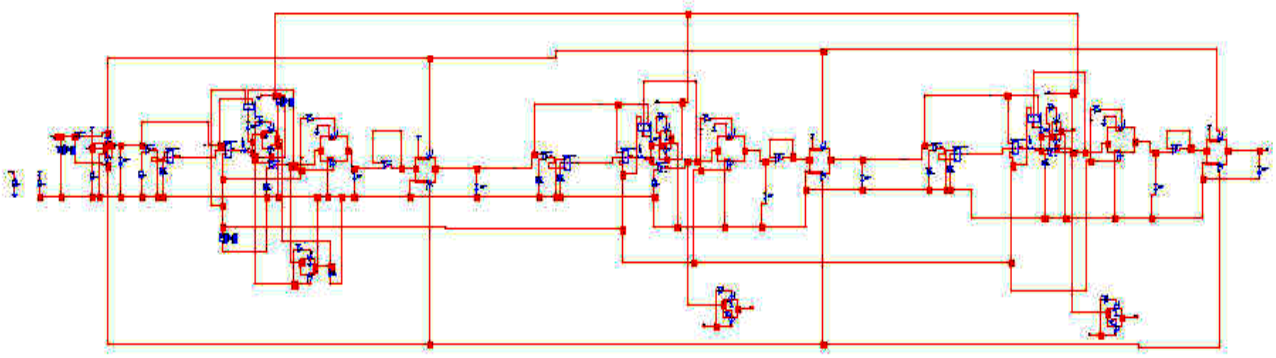


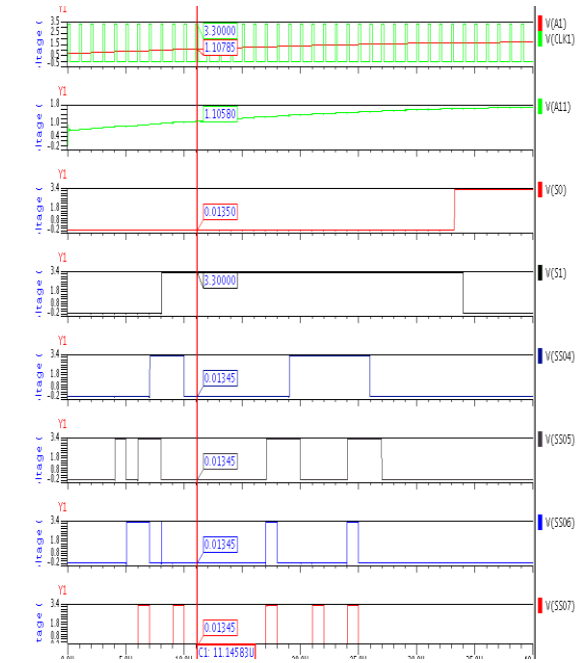
Fig.5 Schematic of 3 bit Analog to Digital Converter

Experimental results of 8 bit digital output are presented on the next page.

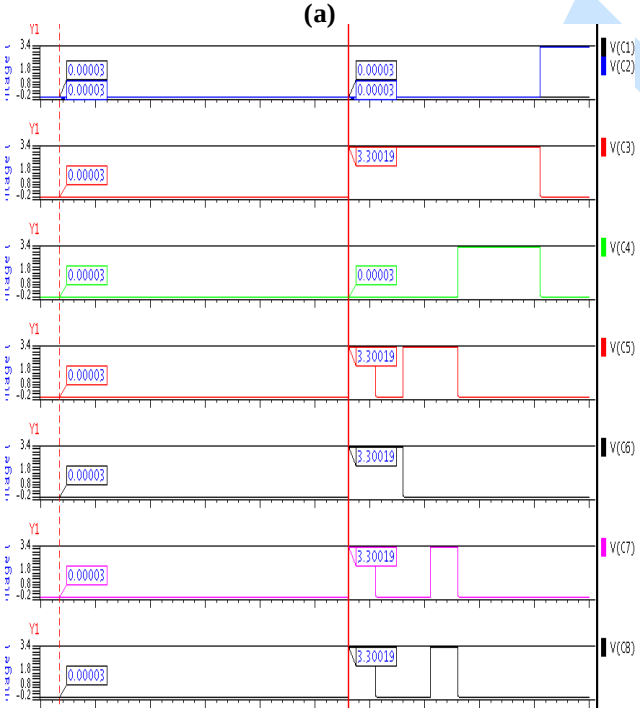
IV. FINAL RESULTS

A complete design & Simulation process of 10 bit Pipelined Analog to Digital Converter with simplified functional blocks modules using 0.35µ tsmc technology is introduced. The above wave forms with sampling frequency 1 MHz show the results of 10 bit ADC with IV signal input. Proposed ADC employing different techniques were simulated using Mat lab to evaluate the impact of the proposed technique on the linearity of ADC. INL = +- 1LSB and DNL =+- 0.5LSB are measured. In each case, various non idealities were considered for the

simulation with focus on the INL and DNL performance. Among them, sampling capacitor mismatch, comparator offset, and finite dc gain were actually taken into account. The INL and the DNL results were obtained through a code density simulation. Further, when proposed capacitor switching technique is employed, the DNL is improved INL is also improved.

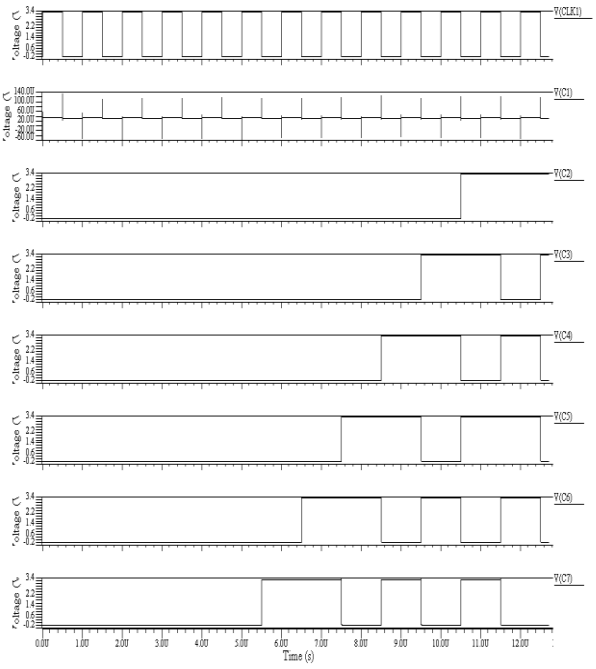


(a)



(b)

Fig.6 8 bit digital Output response for input sine wave



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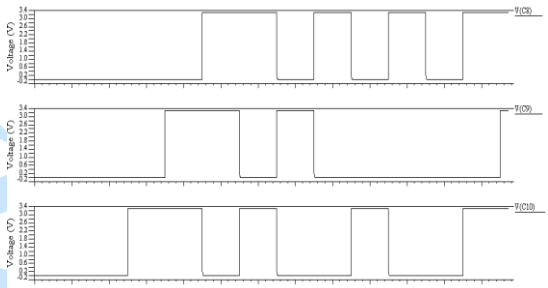

(b)

Fig.7 10 bit digital Output response with I V input sine wave

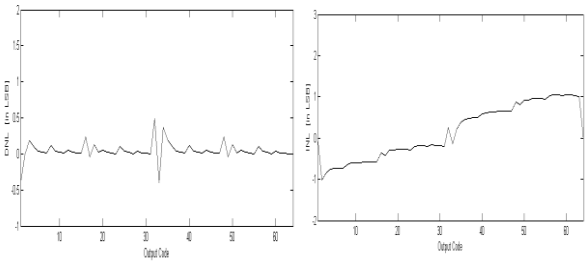

Fig.8 Measurement of DNL and INL

CONCLUSION

This proposed Pipelined ADC architecture is easy to implement with complete circuit realization for low power sensor application.. Here in this block we are using merely 10 operational amplifier and comparator for 10 bit procedure. In this paper, low power technique for biomedical sensor applications is presented. This technique improves both INL and DNL performance due to capacitor mismatch. Behavioral simulation of A/D converter is carried out to evaluate this technique. A study of these provides a better understanding of the design choices

that must be made in low power data converter design.

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